FIG . 1

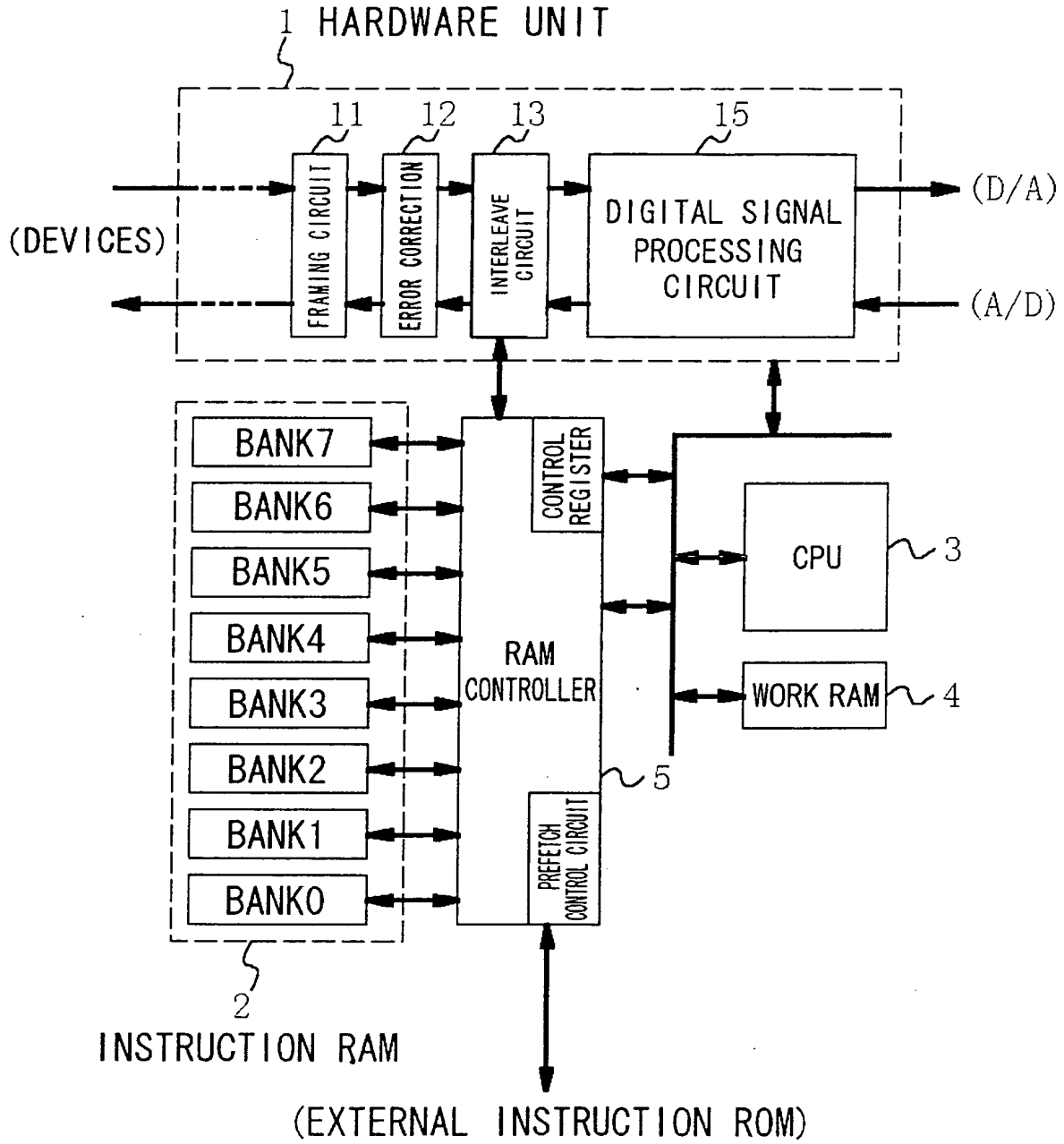
1 HARDWARE UNIT
11
12
13
15
FRAMING CIRCUIT
ERROR CORRECTION
INTERLEAVE CIRCUIT
DIGITAL SIGNAL PROCESSING CIRCUIT
(DEVICES)
(D/A)
(A/D)
BANK7
BANK6
BANK5
BANK4
BANK3
BANK2
BANK1
BANK0
CONTROL REGISTER
RAM CONTROLLER
PREFETCH CONTROL CIRCUIT
5
CPU
3
WORK RAM
4
2
INSTRUCTION RAM
(EXTERNAL INSTRUCTION ROM)

FIG . 2

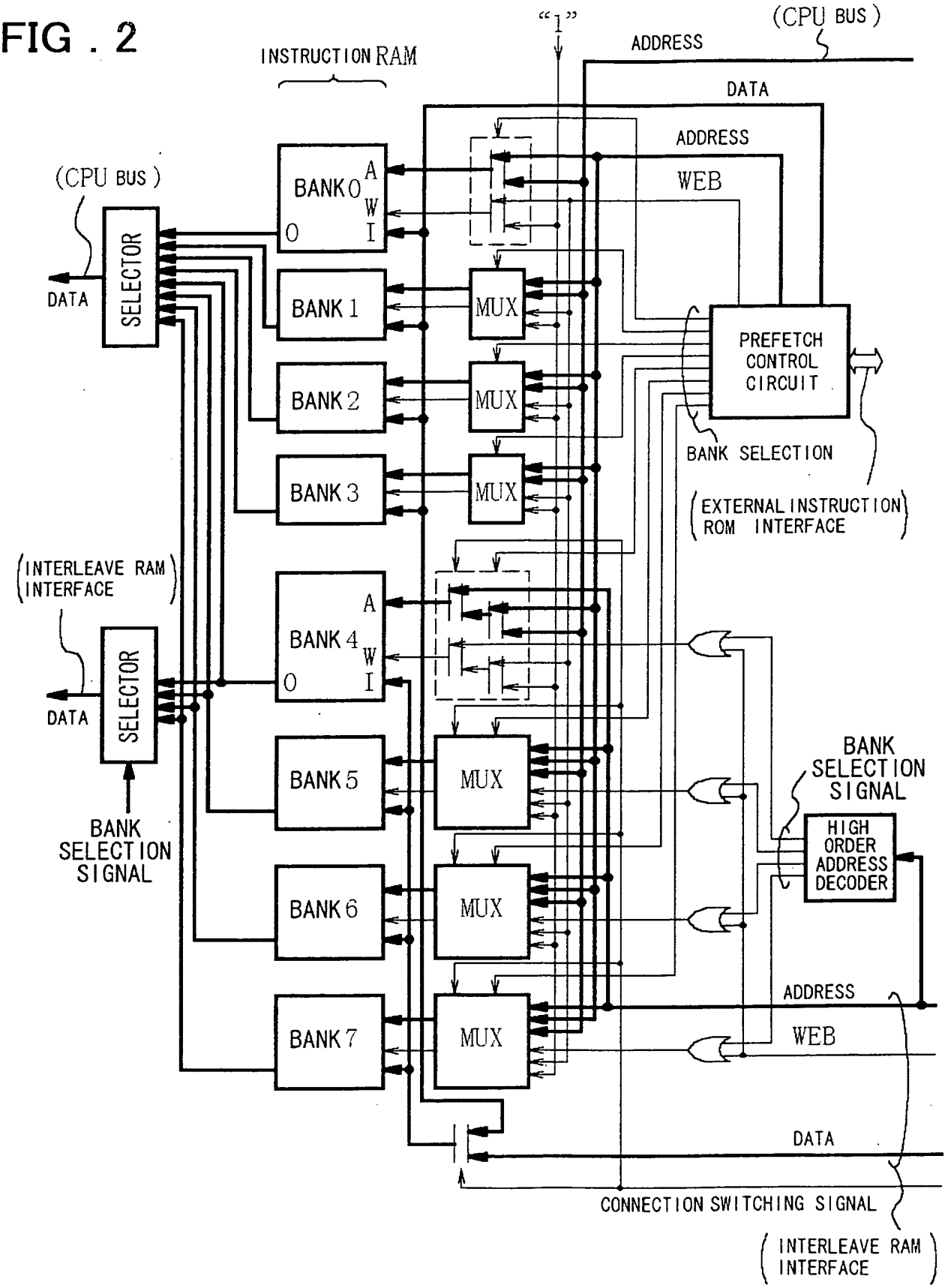
INSTRUCTION RAM
"1"
(CPU BUS)
ADDRESS
DATA
ADDRESS
WEB
(CPU BUS)
BANK 0
A
W
I
0
SELECTOR
DATA
BANK 1
BANK 2
BANK 3
MUX
PREFETCH CONTROL CIRCUIT
BANK SELECTION
(EXTERNAL INSTRUCTION ROM INTERFACE)
(INTERLEAVE RAM INTERFACE)
BANK 4
BANK 5
BANK 6
BANK 7
BANK SELECTION SIGNAL
HIGH ORDER ADDRESS DECODER
ADDRESS
WEB
DATA
CONNECTION SWITCHING SIGNAL
(INTERLEAVE RAM INTERFACE)

FIG . 3(A)

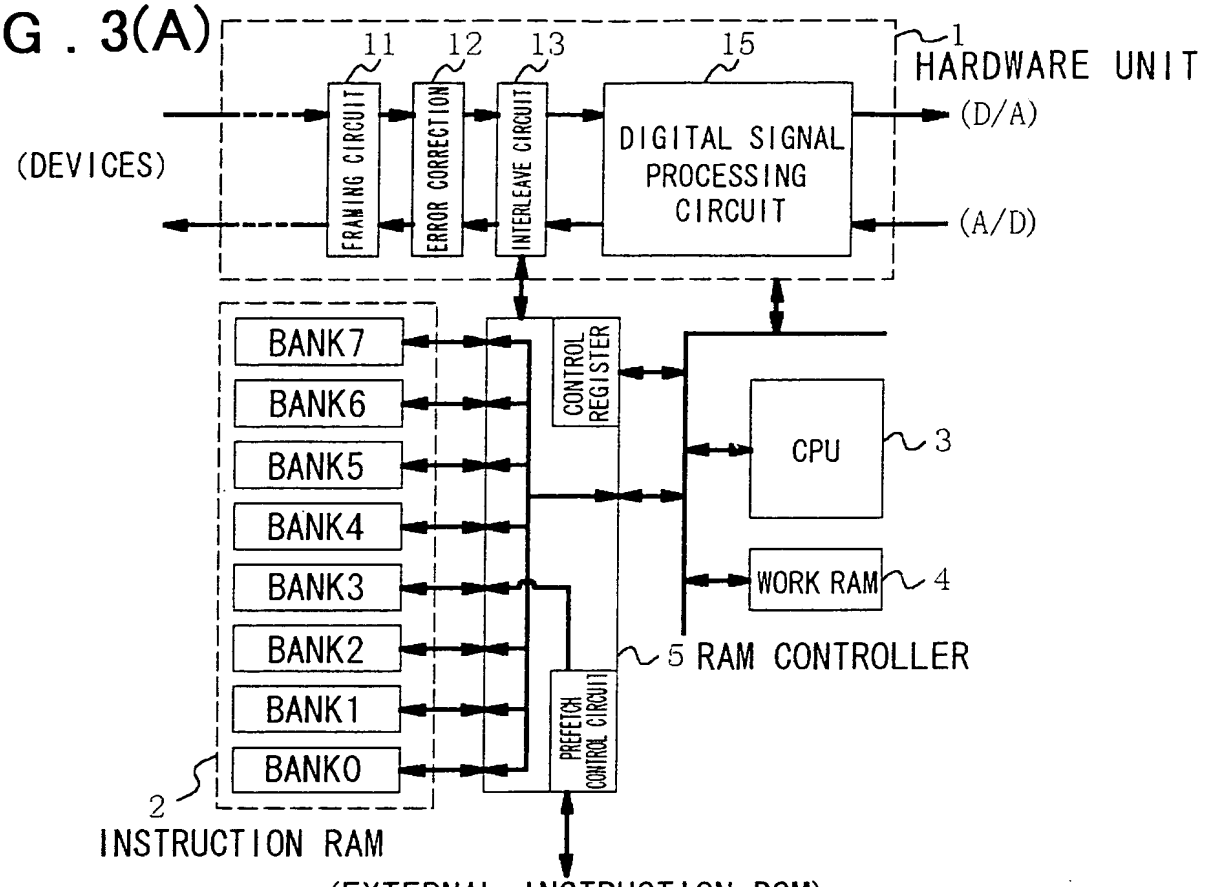

FIG .3(B)

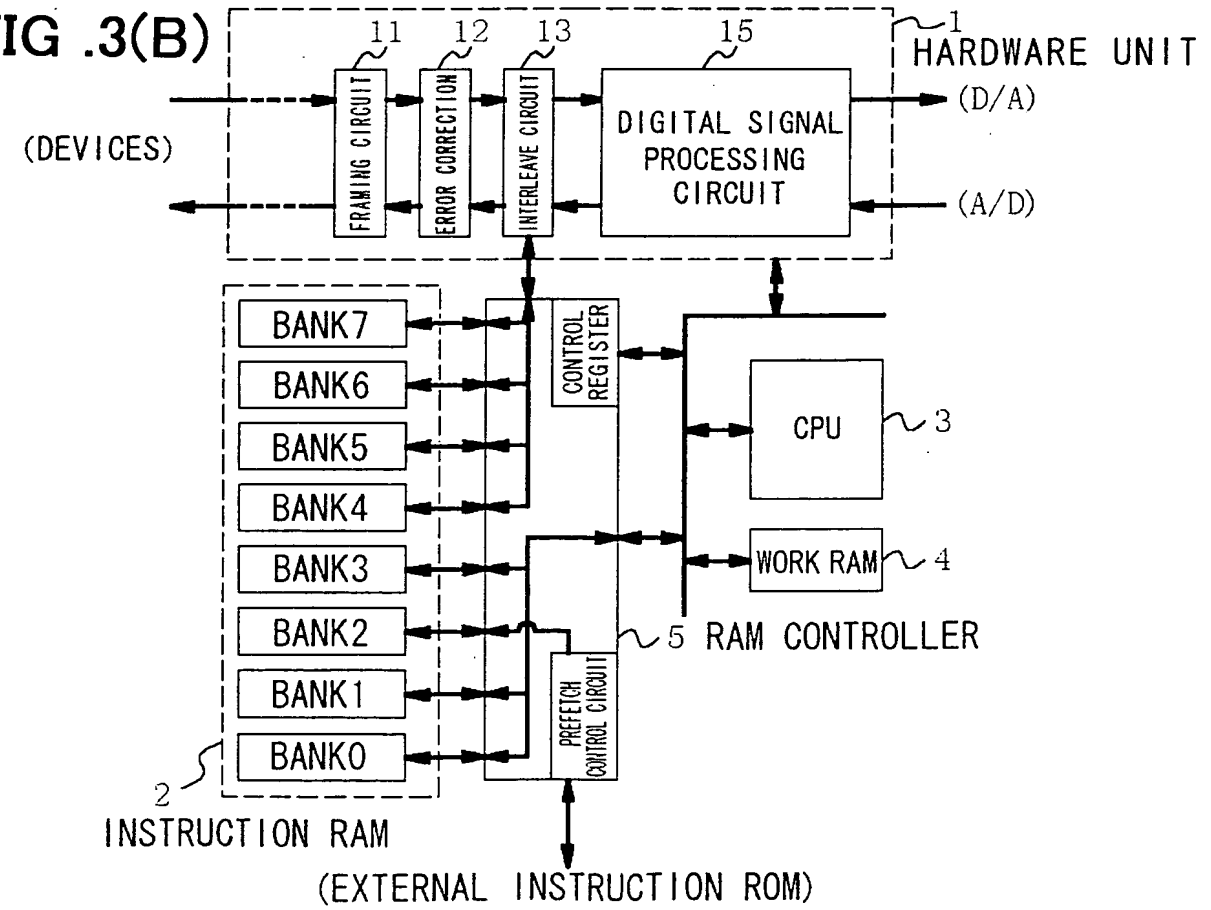

FIG . 4 PRIOR ART